A.2 End

6 ~~8~~. (Amended) An anti-jitter circuit as claimed in claim 2 further including a monostable circuit connected to the output of said means for comparing.

A.3 Sub RS

~~12~~. (Amended) An anti-jitter circuit as claimed in claim 8 wherein said monostable circuit is triggered whenever a discharge part of the time-varying voltage waveform crosses the mean d.c. level.

13. (Amended) An anti-jitter circuit as claimed in claim 1 including frequency doubling means comprising a first said charging means and a second said charging means for deriving charge packets respectively from the rising and falling edges of the input pulse train.

Sub D1

~~14~~. (Amended) An anti-jitter circuit as claim in claim 1 further including means for maintaining the charge value of the charge packets substantially constant.

A.4

Sub D1

~~19~~. (Amended) An anti-jitter circuit as claimed in claim 2 wherein said means for comparing comprises inverted gate means having an input coupled to the integrator charge storage means and an output, and including means defining a further negative feedback path between said output of said inverted gate means and said discharging means whereby to establish said mean d.c. voltage level as a switching level of said inverted gate means.

15 ~~21~~. (Amended) An anti-jitter circuit as claimed in claim ~~19~~ 11 wherein said further negative feedback path comprises a low pass filter.

19 ~~23~~. (Amended) An anti-jitter circuit as claimed in claim 2 wherein said means for comparing comprises inverted gate means having an input coupled to the integrator charge storage means and an output, and including a voltage source coupled to the discharging means whereby to establish said mean d.c. voltage level as a switching level of said inverted gate means.

19 ~~25~~. (Amended) An anti-jitter circuit as claimed in claim 2 including means providing a low impedance path between the input and the output of the negative feedback path.

Cancel claim 28 without prejudice.

- Please add the following new claims 29-30:

13 ~~29~~. (New) An anti-jitter circuit as claimed in claim 12 ~~20~~ wherein said further negative feedback path comprises a low pass filter.

30. (New) An anti-jitter circuit as claimed in claim 29 wherein said low pass filter comprises the combiantion of a resistor and a capacitor.